HIGH-VOLTAGE MIXED-SIGNAL IC

UC1617s

128 x 128 4S STN LCD Controller-Driver

MP Specifications
Revision 1.0

August 24, 2007

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1617s

Single-Chip, Ultra-Low Power
128COM x 128SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1617s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and FRM (Frame Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1617s contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x128 matrix STN LCD with 4 gray shades and B/W Mode.
- A software-readable ID pin and an MTP programmable ID bit to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row ordered and page_c (page column) ordered display buffer RAM access.
- Support industry standard 2-wire, 3-wire, 4-wire serial bus (I^2C, S8, S9) and 8-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates up to 201Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 4 temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command, make RST pin optional.
- Self-configuring 9x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S8, S9, or I^2C) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range (Typ.) : 1.8V ~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.7V ~ 3.3V
  LCD V_{OP} range: 6.0V ~ 15V
- Available MTP trimming support precise LCD contrast matching.
- Available in gold bump dies
  Bump pitch: 26.5 μM
  Bump gap: 12 μM
  Bump surface: 2,001 μM^2

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1617sGAA	Yes	Yes	Gold bumped die with MTP function and I^2C interface

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT SENSITIVITY

The MTP memory cell is sensitive to photon excitation. Under extended exposure to strong ambient light, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light shields to realize full MTP content retention performance.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon. However, unless I^2C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I^2C applications. Unless I^2C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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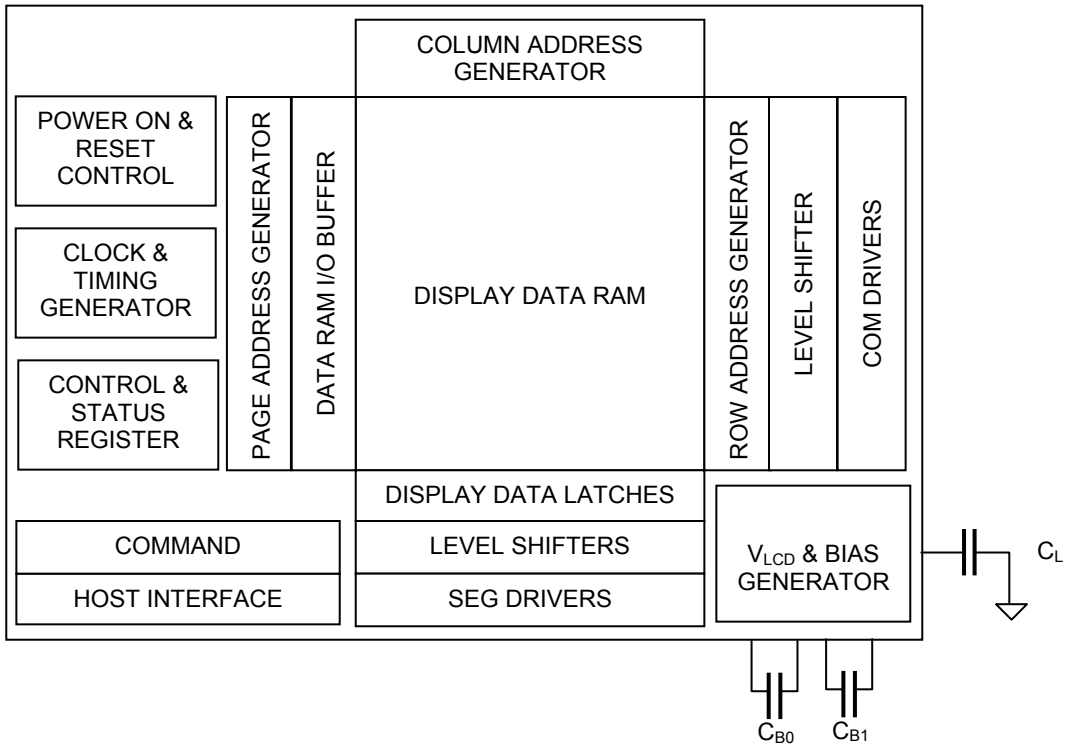
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	1 2 1	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	4 5	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+}, V_{B1-} V_{B0+}, V_{B0-}	PWR	2, 2 2, 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	1 1	High voltage LCD Power Supply. Connect these pins together. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the trace resistance under 50 Ω.

NOTE

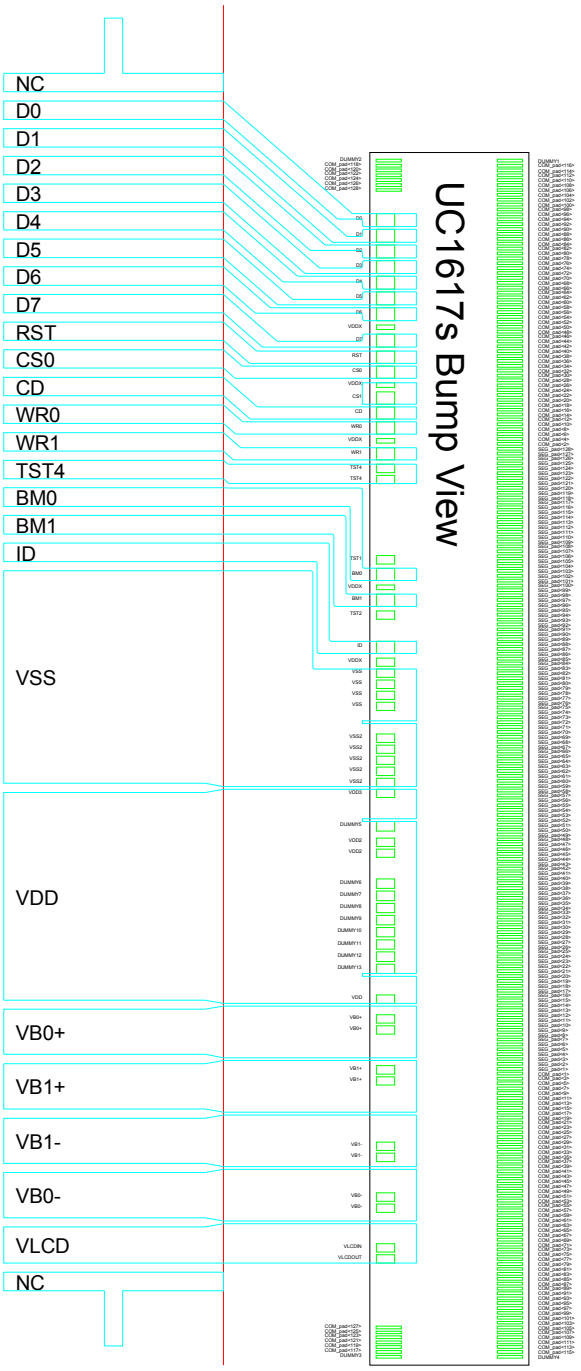
- Recommended capacitor values:
  C_B: 150~250x LCD load capacitance or 2.2μF (5V), whichever is higher.
  C_L: 330nF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7:6]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>11</td><td>2-wire I^2C</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token (S8: conventional)</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token (S9: conventional)</td></tr>
</table></td></tr>
<tr><td>CS0 / A2
CS1 / A3</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.
In I^2C mode, these two pins indicate the I^2C bus address’ bit 2 and bit 3.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1617s has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In I^2C mode, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID</td><td>I</td><td>1</td><td>ID pin is for production control.
The connection will affect the content of PID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>BM=1x (Parallel)</th><th>BM=00 (S8)</th><th>BM=01 (S9)</th><th>BM=01 (I^2C)</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>SKA</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>D7</td><td>D7</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
</table>

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG128	HV	128	SEG (page_c) driver outputs. Support up to 128 pixels. Leave unused drivers open-circuit.
COM1 ~ COM128	HV	128	COM (row) driver outputs. Support up to 128 rows. Leave unused COM drivers open-circuit.
MISC. PINS			
V_{DDX}		5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	2	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage programming power supply for MTP operation. For COG design with MTP options, please wire out TST4 with an ITO trace resistance 30 ~ 70 Ω.
TST1 TST2	I/O	1 1	Test I/O pin. Leave these pins open during normal use.
Dummy		13	Dummy pins are NOT connected inside the IC.

Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*x* or SEG*x* will correspond to index *x*-1, and the value ranges for those index registers will be 0~127 for COM and 0~127 for SEG.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1617s, V_{DD}=1.8V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20 Ω or lower; otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below 1.65V during high speed data-write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1617s contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1617s will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections, 2xFLT on one side non-scrollable, 2XFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CR	5	00H	Return Page_C Address. Useful for cursor implementation.
CA	5	00H	Display Data RAM Page_C Address (Used in Host to Display Data RAM access)
RA	7	00H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 6 01b: 9 10b: 10 **11b: 11**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.00%** 01b: -0.10% 10b: -0.15% 11b: -0.05%
PM	8	4EH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	--	PM offset. PMO[5] = 1: The effective PM value, PMV = PM – PMO[4:0] PMO[5] = 0: The effective PM value, PMV = PM + PMO[4:0]
PC	4	EH	Power Control. PC[1:0]: 00b: LCD: ⩽ 6nF 01b: LCD: 6~9nF **10b: LCD: 9~13nF** 11b: LCD: 13~18nF PC[3:2]: 00b: External V_{LCD} **11b: Internal V_{LCD} (9X pump, standard)**
DC	4	8H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray Shade and B/W mode 0b: B/W Mode **1b: 4-Shade Mode**

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>AC</td><td>4</td><td>01H</td><td>Address Control:
AC[0]: WA: Automatic page_c/row Wrap Around (Default 1: ON)
AC[1]: Auto-Increment order
0: Page_C (CA) first 1: Row (RA) first
AC[2]: RID: RA (Row Address) auto increment direction (L:+1 H:-1)
AC[3]: Window Program Enable
0 : Disable 1 : Enable</td></tr>
<tr><td>LC</td><td>11</td><td>008H</td><td>LCD Control:
LC[0]: Enable the first FLx2 lines in partial display mode (Default OFF).
LC[1]: MX, Mirror X. SEG/Page_C sequence inversion (Default: OFF)
LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: OFF)
LC[4:3]: Line Rate (Klps: Kilo-line-per-second)
00b: 14.2 Klps 01b: 17.3 Klps
10b: 21.1 Klps 11b: 25.7 Klps
Line Rate (for On/Off mode):
00b: 5.7 Klps 01b: 7.0 Klps
10b: 8.5 Klps 11b: 10.4 Klps
(Line-Rate = Frame-Rate * Mux-Rate)
LC[8:5]: Gray-Shade control.
<table><tr><th>LC[6:5]</th><th>Gray-shade Level</th><th>LC[8:7]</th><th>Gray-shade Level</th></tr><tr><td>00</td><td>1</td><td>00</td><td>3</td></tr><tr><td>01</td><td>2</td><td>01</td><td>4</td></tr><tr><td>10</td><td>3</td><td>10</td><td>5</td></tr><tr><td>11</td><td>4</td><td>11</td><td>6</td></tr></table>LC[10:9]: Partial Display Control
0xb: Disable Mux-Rate = CEN+1 (DST, DEN not used)
11b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB)
x 2</td></tr>
<tr><td>NIV</td><td>4</td><td>6H</td><td>N-line Inversion:
NIV[1:0]: 00b: 9 lines 01b: 13 lines
10b: 17 lines 11b: 23 lines
NIV[2]: 0b: no-XOR 1b: XOR
NIV[3]: 0b: NIV Disabled 1b: NIV Enabled</td></tr>
<tr><td>CEN
DST
DEN</td><td>7
7
7</td><td>7FH
00H
7FH</td><td>COM scanning end (last COM with full line cycle, 0 based index)
Display start (first COM with active scan pulse, 0 based index)
Display end (last COM with active scan pulse, 0 based index)
Please maintain the following relationship:
CEN = the actual number of pixel rows on the LCD - 1
CEN ⩾ DEN ⩾ DST+ 9</td></tr>
<tr><td>WPC0</td><td>5</td><td>00H</td><td>Window program starting page_c address. Value range: 0 ~31.</td></tr>
<tr><td>WPP0</td><td>7</td><td>00H</td><td>Window program starting row Address. Value range: 0~127.</td></tr>
<tr><td>WPC1</td><td>5</td><td>1FH</td><td>Window program ending page_c address. Value range: 0~31.</td></tr>
<tr><td>WPP1</td><td>7</td><td>7FH</td><td>Window program ending row Address. Value range: 0~127.</td></tr>
</table>

Name	Bits	Default	Description
MTPC	6	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : Idle 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip use only. MTPC[3] : MTP Enable (auto clear after MTP command action done) MTPC[4] : Use/Ignore MTP value. 0: Ignore **1: Use** MTPC[5] : For testing only. Set to 0 for normal operation.
MTP	8	–	Multiple-Time Programming. MTP[5:0] for V_{LCD} fine tune MTP[7:6] for LCM manufacturer's configuration.
MTPM	6	00H	MTP Write Mask. 01H: program, **00H: no action**.
APC [2:0]	–	N/A	Advanced Product Configuration. For UltraChip only. Do *NOT* use.
Status Register			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag : 1 - MTP version, 0 - non-MTP version
MS	1	–	MTP programming in-progress
WS	1	–	MTP Command Succeeded
ID	1	PIN	Access the connected status of ID pin.
Get Status Sequence			
MX, MY, WA, DE, WS, MD, MS	1, 1, 1, 1 1, 1 1	1st	MX : Mirror X, LC[1] MY : Mirror Y, LC[2] WA : Wrap Around, AC[0] DE : Display Enable WS : MTP Succeeded MD : MS : MTP Status
Ver, PMO	2, 6	2nd	Ver : IC Version, range 00~-01, default : 0 PMO : PM Offset, PMO[5:0]
Prod_Code, PID	4, 1	3rd	Prod_Code [3:0], default = 7H, PID

COMMAND SUMMARY

The following is a list of host commands supported by UC1617s

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	-	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Prod_Code, PID}	N/A
				Ver		PMO[5:0]							
				Prod_Code				0	PID	0	0		
4.	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	00H
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1 or 2	N/A
		0	0	#	#	#	#	#	#	#	#		
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10.	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0H
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0H
11.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	4EH
		0	0	#	#	#	#	#	#	#	#		
12.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[10:9]	00b: Disable
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	00H
				#	#	#	#	#	#	#	#		
15.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18.	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[3:0]	6H
				-	-	-	-	#	#	#	#		
21.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	01b
22.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[8:7]	10b
23.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
26.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
27.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
30.	Set Window Program Starting Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	0 #	0 #	Shared with MTP commands	Set WPC0	0
31.	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
32.	Set Window Programming Ending Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	1 #	0 #		Set WPC1	31
33.	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
34.	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Disable
35.	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
36.	Set MTP Write Mask	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[5:0]		0
37.	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
38.	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	
39.	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	
40.	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	
SERIAL READ COMMAND (ENABLED ONLY IN S8/S9 MODE)														
41.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status until chip disabled		N/A
		0	1	-	MX	MY	WA	DE	WS	MD	MS			
		0	1	Ver		PMO[5:0]								
		0	1	Prod_Code				0	PID	0	0			

Notes:

- Any bit patterns other than the commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on register MTPC[3].
- Commands (37)~(40) are shared with commands (30)~(33) and have exactly the same code. When MTPC[3]=0, commands (37)~(40) are interpreted as `Window Programming` commands. When MTPC[3]=1, they are the `MTP Control` commands.
- MTPM and PM are actually the same register. Only one of the commands (36 or 11) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Row Address register (RA) and Page_C Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each page_c of pixel corresponds to one page_c of SRAM data. RA and CA registers can be programmed by issuing `Set row Address` and `Set Page_C Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of page_c address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (PID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 31), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	**-**	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]	PMO[5:0]						
			Product Code				**0**	PID	**0**	**0**

Status 1 definitions:
- *MX*: Status of register LC[1], mirror X.
- *MY*: Status of register LC[2], mirror Y.
- *WA:* Status of register AC[0]. Automatic page_c/row wrap around.
- *DE*: Display enable flag. DE=1 when display is enabled
- *WS*: MTP Command Succeeded
- *MD*: MTP Option (1 - MTP version, 0 - non-MTP version)
- *MS*: MTP action status

Status 2 definitions:
- *Ver[1:0]*: IC Version Code, 00 ~ 11. Default: 00
- *PMO[5:0]:* PM offset value

Status 3 definitions:
- *Prod_Code:* 0111b (7h)
- *PID:* Provide connection status of accessing to ID pin.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page_C Address LSB CA[4:0]	0	0	**0**	**0**	**0**	CA4	CA3	CA2	CA1	CA0

Set SRAM page_c address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~31

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b= -0.00%/°C 01b= -0.10%/°C 10b= -0.15%/°C 11b= -0.05%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b≤6nF 01b=6~9nF **10b=9~13nF** 11b=13~18nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External V_{LCD} **11b= Internal V_{LCD}** (9X pump, standard)

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC register parameter							

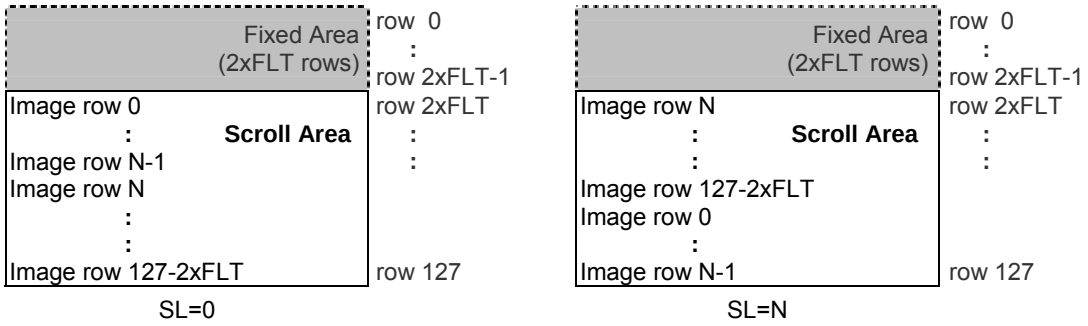
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by `Set Fixed Lines` command.



(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address RA [6:4]	0	0	**0**	**1**	**1**	**1**	**-**	RA6	RA5	RA4

Set SRAM row Address for read/write access.

Possible value = **0**~127

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 193**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [10:9]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC10	LC9

This command is used to enable partial display function.

LC[10:9] : **0xb: Disable Partial Display**, Mux-Rate = CEN+1 (DST, DEN not used.)
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic page_c/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increase by one.

AC[1]: Auto-Increment order
0 : page_c (CA) increase (+1) first until CA reaches CA boundary, then RA will increase by (+/-1).
1 : row (RA) increase (+/-1) first until RA reach RA boundary, then CA will increase by (+1).

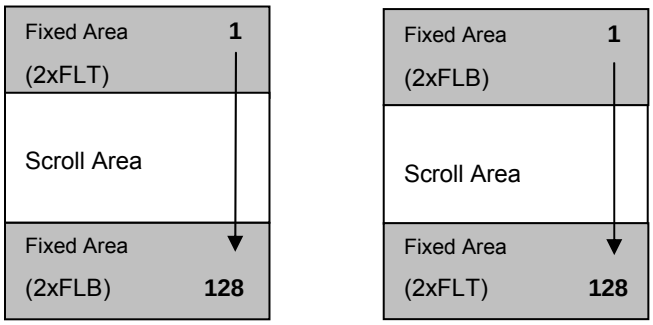
AC[2]: RID, Row Address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether row Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[3]=ON), see Command Description (31) ~ (35) for more details. When Window Program is disabled (AC[3]=OFF), the behavior of CA, RA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[3]=ON.

(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate * Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 85, 64, 43, and 32.

The followings are line rates at Mux Rate = 86~128:

00b: 14.2 Klps 01b: 17.3 Klps 10b: 21.1 Klps 11b: 25.7 Klps
(Klps: Kilo-Line-per-second)

while the followings are line rates in On/Off mode:

00b: 5.7 Klps 01b: 7.0 Klps 10b: 8.5 Klps 11b: 10.4 Klps

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(18) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	DC3	DC2

This command is for programming register DC[3:2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit, and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1617s will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3]: Gray Shade and B/W mode
0b: B/W Mode **1b: 4-Shade Mode**

For B/W mode, use data format for 4-shade-mode and UC1617s will convert them for B/W mode automatically.

Note : When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1617s for 5~10mS after setting DC[2] to 1.

(19) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] for COM (row) mirror (MY), SEG (page_c) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 31-CA as write/read (from host interface) display RAM page_c address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

(20) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [3:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(Double-byte command)	0	0	**-**	**-**	**-**	**-**	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[5:0] for N-Line Inversion:

NIV[1:0]: 00b: 9 lines 01b: 13 lines
10b: 17 lines 11b: 23 lines
NIV[2]: 0b: no-XOR **1b: XOR**
NIV[3]: **0b: Disable NIV** 1b: Enable NIV

(21) SET LCD GRAY SHADE 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[6:5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	LC6	LC5

This command sets gray scale register (LC[6:5]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[6:5]: Select Gray-shade
00b: 1 **01b: 2** 10b: 3 11b: 4

LC[6:5]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	1	9
01b	2	12
10b	3	15
11b	4	21

(22) SET LCD GRAY SHADE 2

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[8:7]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC8	LC7

This command sets gray scale register (LC[8:7]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[8:7]: Select Gray-shade
00b: 3 01b: 4 **10b: 5** 11b: 6

LC[8:7]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	3	15
01b	4	21
10b	5	24
11b	6	27

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for "no operation".

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:
00b = 6 01b = 9 10b = 10 **11b = 11**

***(27)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(double-byte command)	0	0	**-**	*CEN [6:0]* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

***(28)* SET DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(double-byte command)	0	0	**-**	*DST [6:0]* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

***(29)* SET DISPLAY END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(double-byte command)	0	0	**-**	*DEN [6:0]* register parameter						

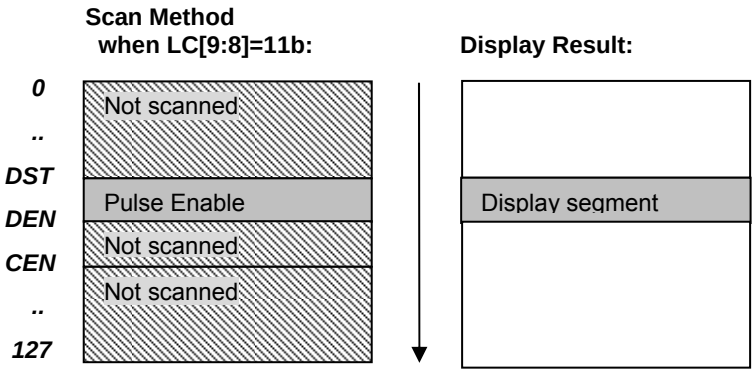
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

CEN, DST DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9:8]=11b, the Mux-Rate is narrowed down to DST-DEN+1 + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use B/W mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(30) SET WINDOW PROGRAM STARTING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	**-**	**-**	**-**	*WPC0[4:0]* register parameter				

This command is to program the starting page_c address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	**-**	*WPP0[6:0]* register parameter						

This command is to program the starting row Address of RAM program window.

(32) SET WINDOW PROGRAM ENDING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	**-**	**-**	**-**	*WPC1[4:0]* register parameter				

This command is to program the ending page_c address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	**-**	*WPP1[6:0]* register parameter						

This command is to program the ending row Address of RAM program window.

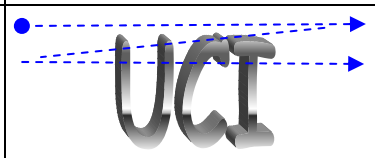
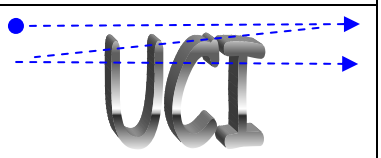
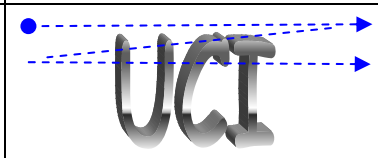
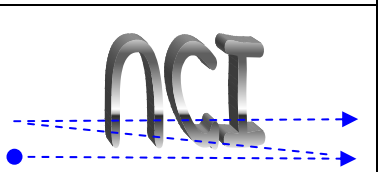
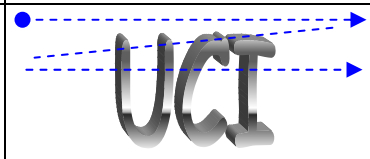
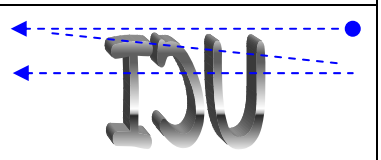
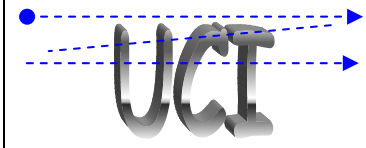
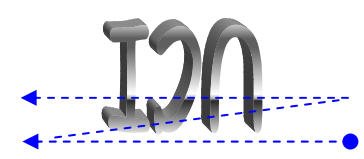
(34) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]) , PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row / page_c after reaching the specified window page_c / row boundary. PID controls the RAM address increasing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM page_c address increasing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

Display Data Direction	Function Setting			Image in the Host (MPU) (Start : ●)	Image in Display Data Ram (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]		
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		

(35) SET MTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	*MTPC* register parameter					

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)
MTPC[5] : For testing only. Set to 0 for normal operation.

The following commands (36~40) are only valid when MTPC[3] =1:

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(36) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	**-**	*MTPM[5:0]* register parameter					

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[5:0]: Set PMO value

This command is only valid when MTPC[3]=1.

(37) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{MPT1} (use with BR=00) and is only valid when MTPC[3]=1.

(38) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} (use with BR=10) and is only valid when MTPC[3]=1.

(39) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(40) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

Serial Read Command (Enable only in S8/S9 mode):

(41) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	1	1	1	1	1	1	1	0
	0	1	-	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]		PMO[5:0]					
			Prod_Code				**0**	PID	**0**	**0**

Please refer to command (3).

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1617s via registers CEN, DST, DEN, and partial display control LC[9:8].

Combined with low power partial display mode and a low bias ratio of 6, UC1617s can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$BR = V_{LCD}/V_{BIAS}$,
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to loose visibility.

UC1617s supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	9	10	11

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{O}C	-0.00	-0.10	-0.15	-0.05

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

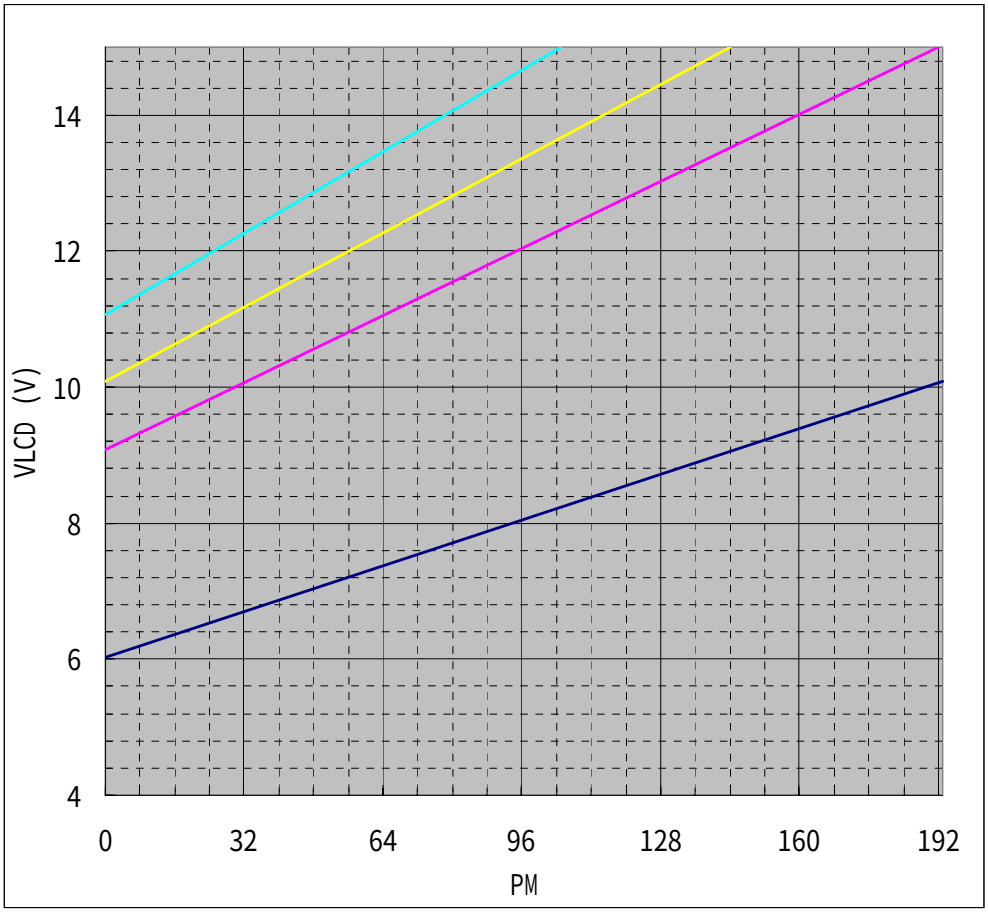
Gray shade LCD is sensitive to even a 1.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1617s is designed to handle LCD panels with load capacitance up to ~15nF when V_{DD2} = 2.7V. 15nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher V_{DD}.

V_{LCD} QUICK REFERENCE



V_{LCD} Relationship to BR and PM at 25 °C

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} (V)
6	6.027	21.00	0	6.03
			193	10.08
9	9.083	30.82	0	9.08
			192	15.00
10	10.079	34.14	0	10.08
			144	15.00
11	11.070	37.41	0	11.07
			105	15.00

Note:

1. For good product reliability, keep $V_{LCD\ (max)}$ under **15.0V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

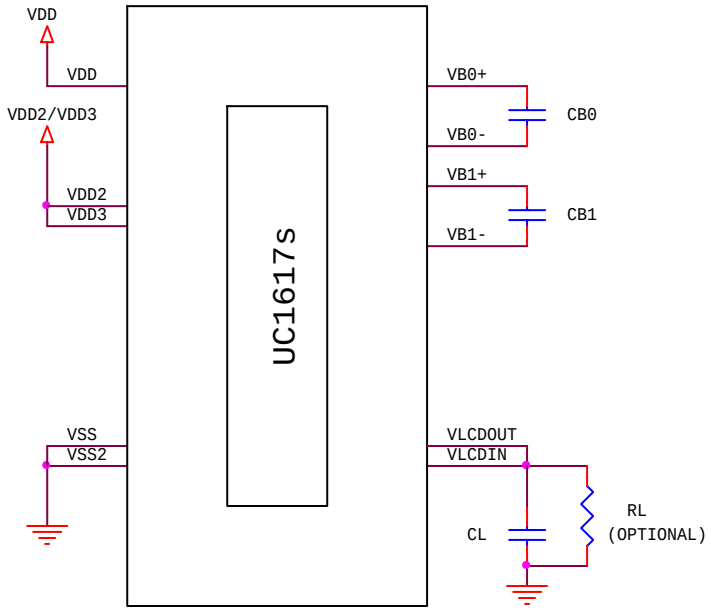


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

- Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)
  C_B: 150 ~ 250x LCD load capacitance or 2.2μF (5V), whichever is higher.
  C_L: 330 nF (25V) is appropriate for most applications.
  R_L: 3.3M Ω ~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1617s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 86, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 85, 64, 43 and 32, line rate will be scaled down by 1.5, 2, 3 and 4 times automatically reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with $(t_r + t_f)$ < 160mS is used, faster line rate may be required under 4-shade mode to maintain good contrast ratio at operating temperature >50^{o}C.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~128, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1617s will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1617s will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1617s provides flexible control of Mux Rate and active display area. Please refer to Command Description (28) ~ (30) for more detail.

GRAY-SHADE MODULATION

UC1617s uses a proprietary line rate modulation scheme to generate 8 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[7:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1617s can be as short as 30μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

COM TRACE

Excessive RC decay of COM scanning pulse can cause fluctuation of contrast and increase the crosstalk of COM direction.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 1.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 0.44\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

SEG TRACE

Excessive RC decay of SEG signal can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel page_c. It can be calculated by C_{LCD}/#_page_c, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one page_c of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/128	1/11	8.98%	7.2%	6.5%
1/128	1/10	8.79%	7.0%	6.3%

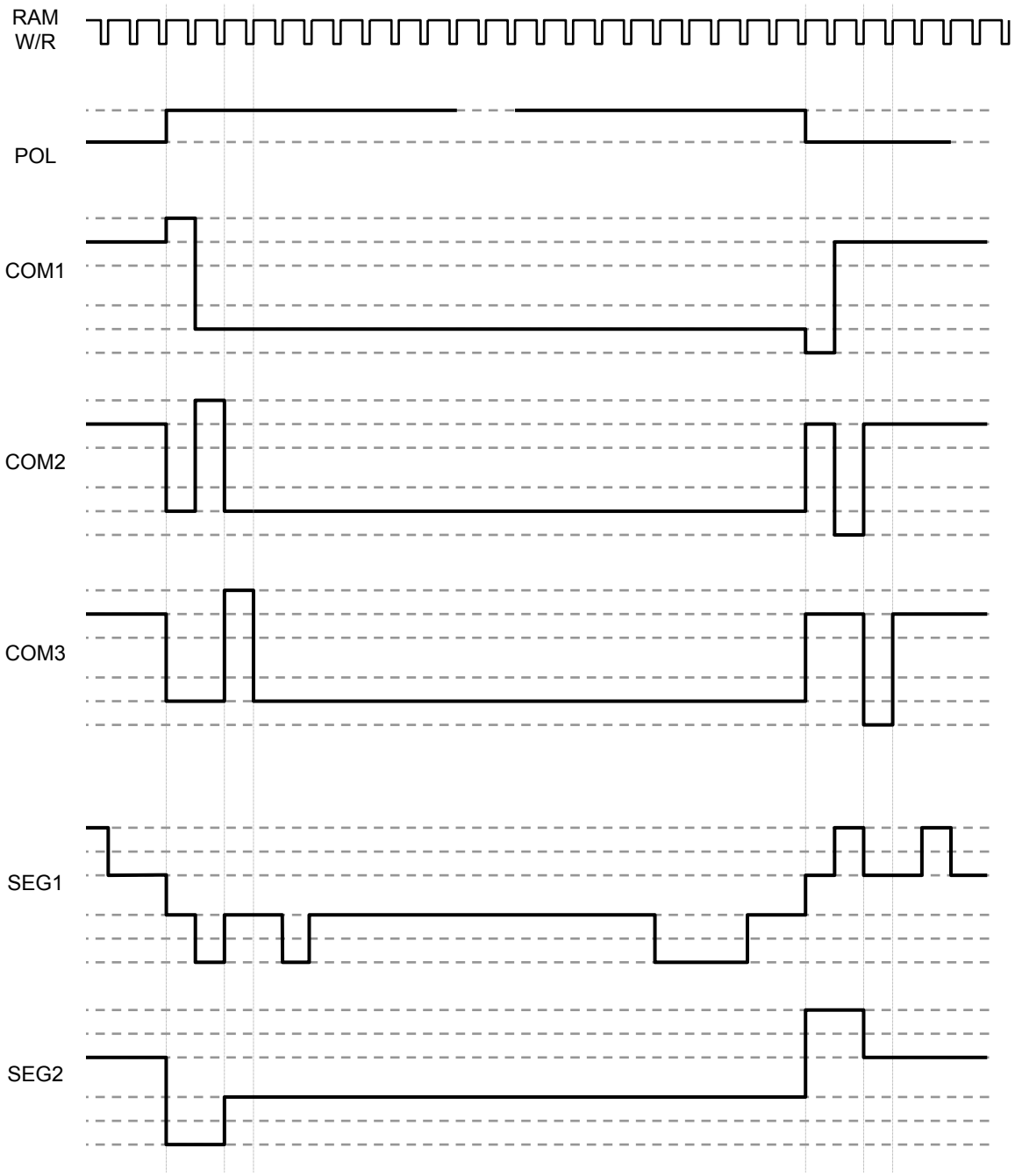


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1617s supports two parallel bus protocols in 8-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type				
		8080	**6800**	**S8 (4-wire)**	**S9 (3-wire)**	**I^2C (2-wire)**
Width		8-bit	8-bit	Serial		
Access		Read/Write		Write Only		R/W
Control & Data Pins	BM[1:0]	10	11	00	01	01
	D[7:6]	Data	Data	10	10	11
	CS[1:0]	Chip Select				A[3:2]
	CD	Control/Data				–
	WR0	$\overline{WR}$	R/$\overline{W}$	0	0	0
	WR1	$\overline{RD}$	EN	0	0	0
	D[5:4]	Data	Data	–		
	D[3:0]	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}.

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1617s internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, by either `Set CA`, or `Set RA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT BUS OPERATION

UC1617s supports both 8-bit bus width.

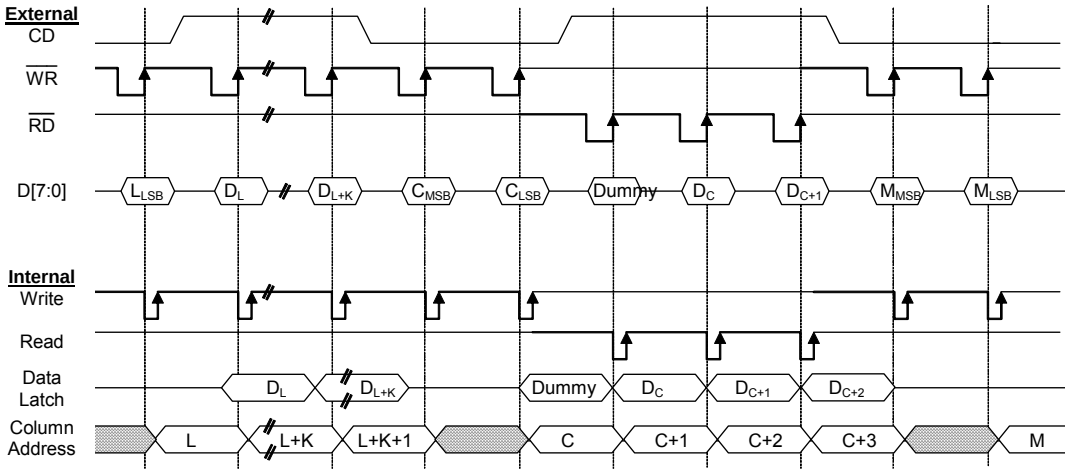


FIGURE 3: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1617s supports three serial modes, one 4-wire SPI mode (S8), one compact 3-wire mode (S9) and one 2-wire mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

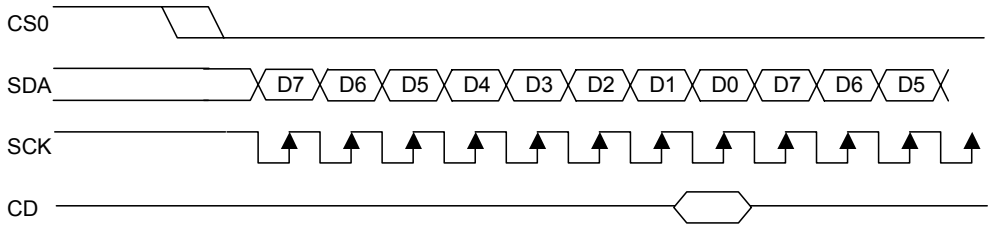


FIGURE 4.a: 4-wire Serial Interface (S8)

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

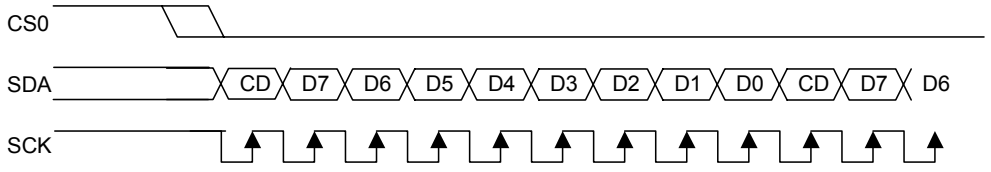


FIGURE 4.b: 3-wire Serial Interface (S9)

2-WIRE SERIAL INTERFACE (I^2C)

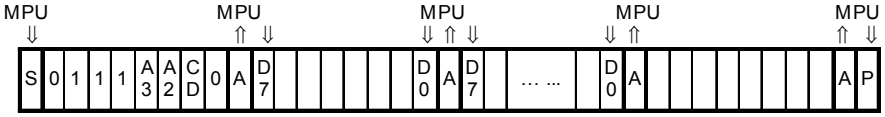
When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1617s is configured as an I^2C bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1617s' device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^2C mode.

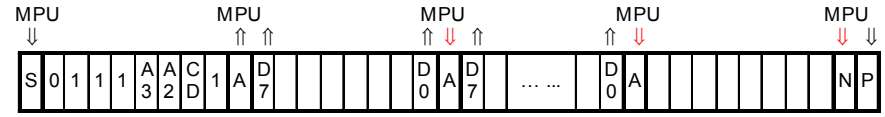
Each UC1617s I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^2C mode and should be connected to V_{SS}.

Write Mode



Read Mode

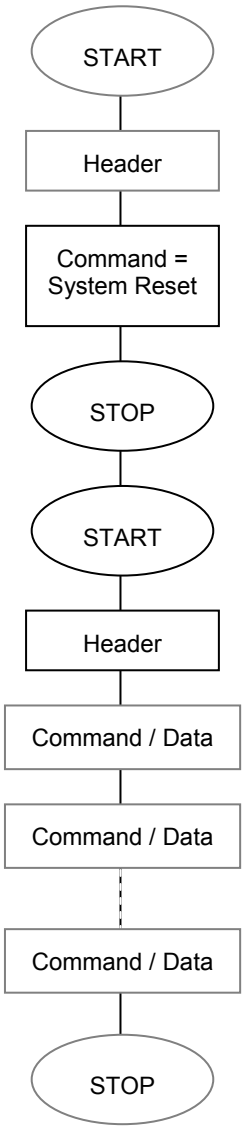


The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1617s will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1617s) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

When using I^2C serial mode, if the command of System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a “System Reset” command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

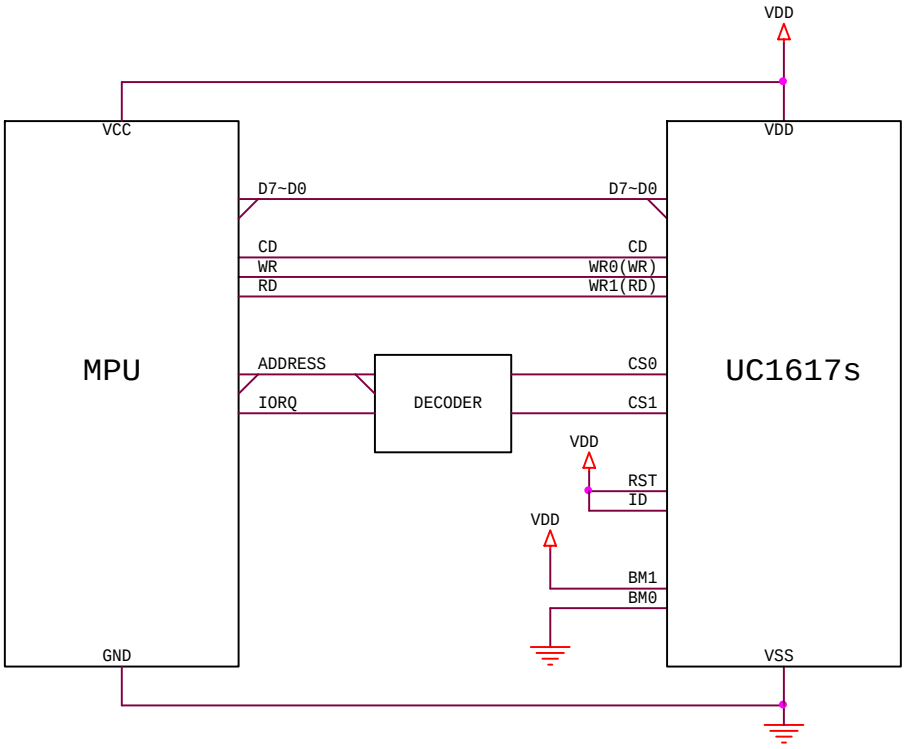


FIGURE 5: 8080/8bit parallel mode reference circuit

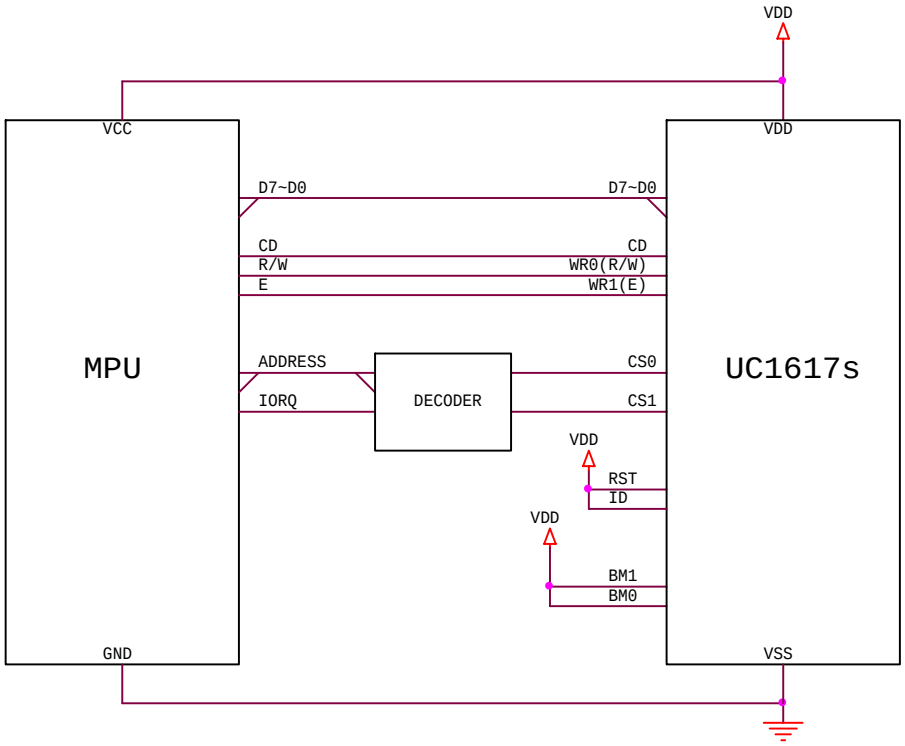


FIGURE 6: 6800/8bit parallel mode reference circuit

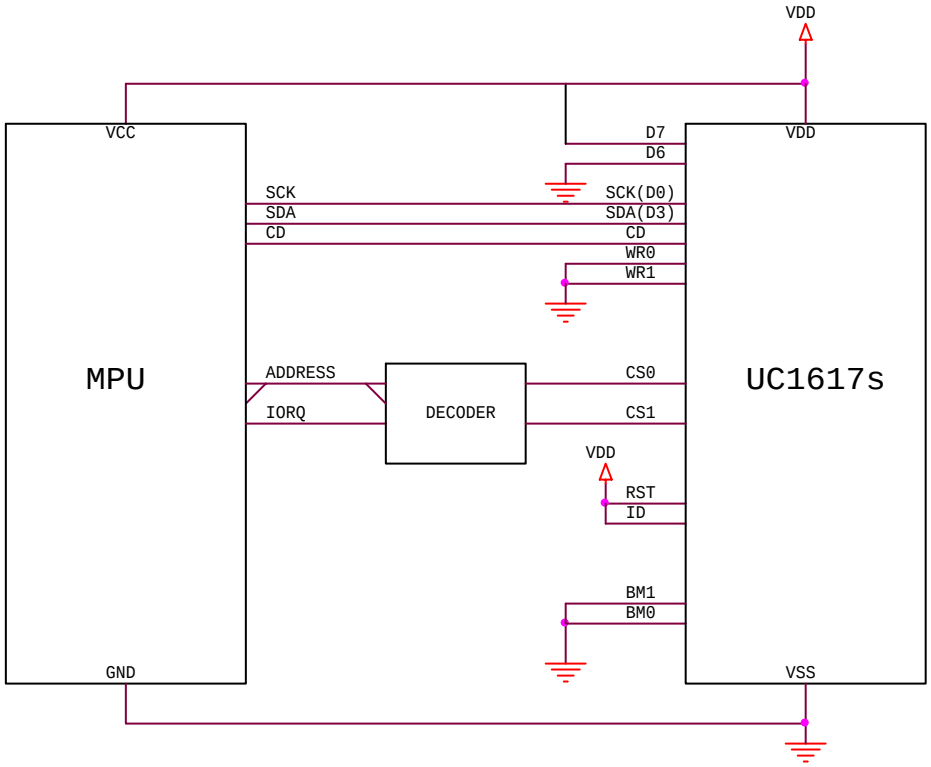


FIGURE 7: 4-Wires SPI (S8) serial mode reference circuit

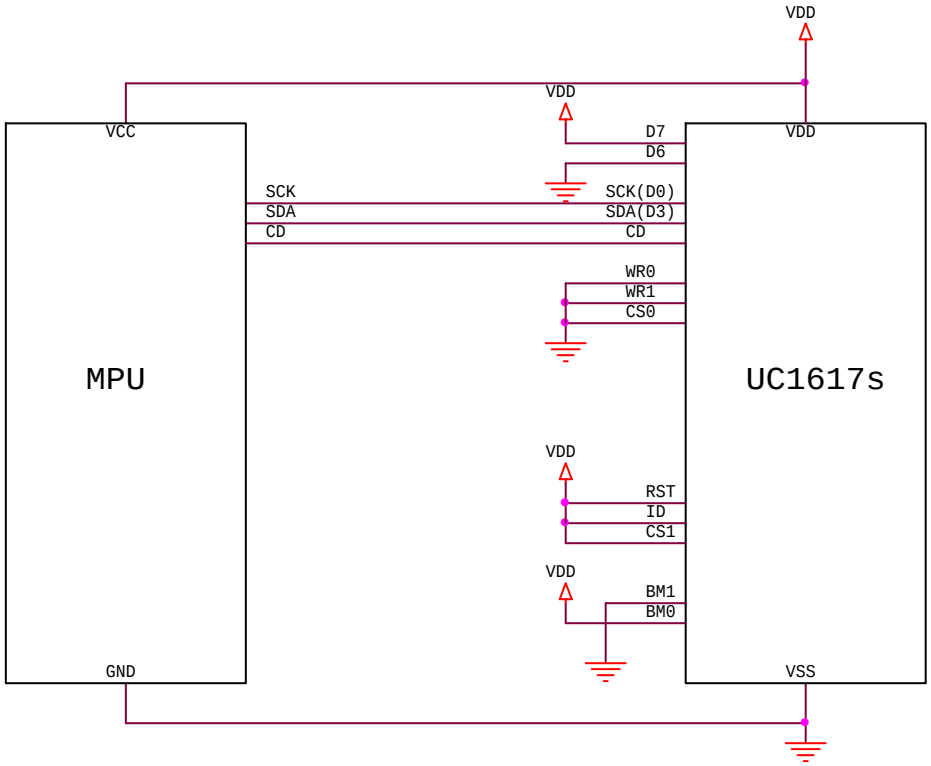


FIGURE 8: 3/4-Wires SPI (S9) serial mode reference circuit

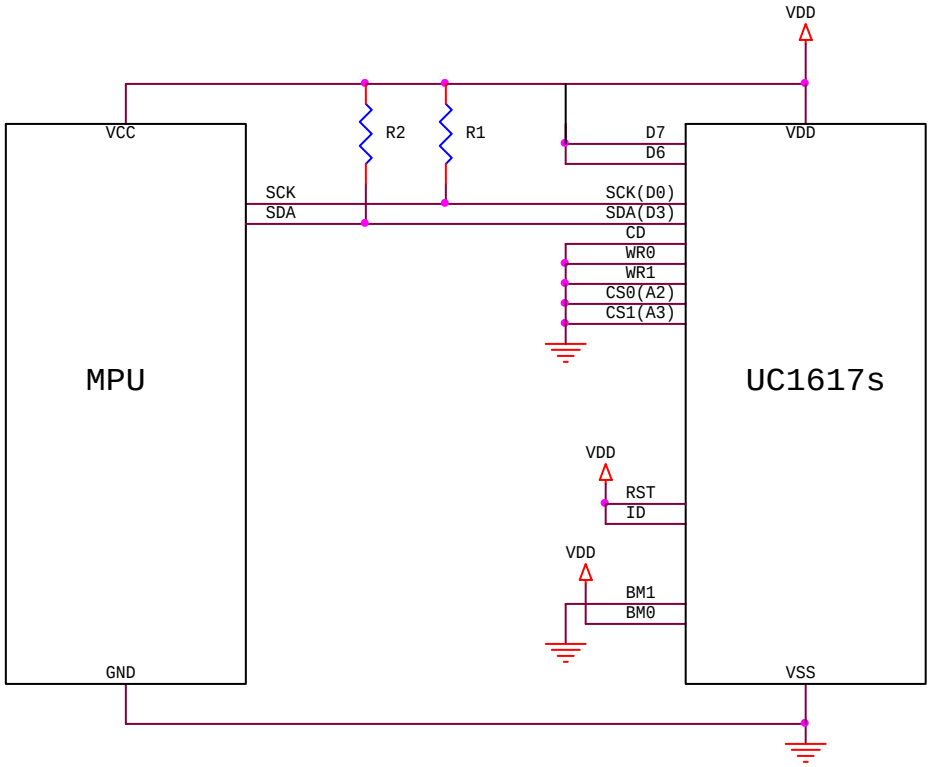


FIGURE 9: I^2C serial mode reference circuit

Note

- The ID pin is for production control. The connection will affect the content of PID of the 3rd byte of `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.
- When using I^2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x128x2.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its page_c and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Page_C Address (CA) by issuing `Set Row Address` and `Set Page_C Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (127), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches end of row, CA will be reset to 0 and RA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Page_C Mirroring (MX) is implemented by selecting either (CA) or (31–CA) as the RAM page_c address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 128)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *128*. Effects such as row scrolling, row swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *128*)
where MUX = CEN + 1

Otherwise
Line = Mod(*Line-1* , *128*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

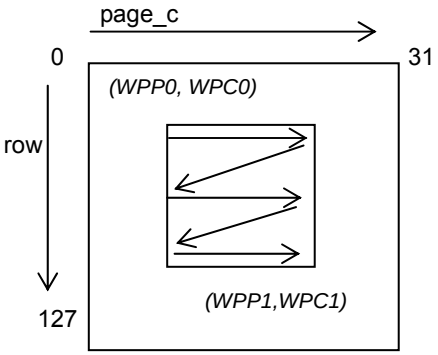
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[3]. After AC[3] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either page_c or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial page_c address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

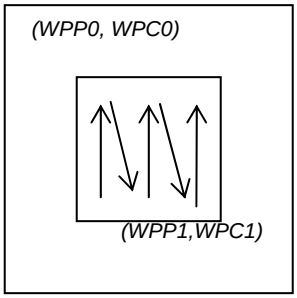
Example1:

AC[2:0] = 001 MX=0



Example 2:

AC[2:0] = 111 MX = 0



RAM

Line Adderss	Data	D1 / 0	D3 / 2	D5 / 4	D7 / 6	D1 / 0	D3 / 2	D5 / 4	D7 / 6		D1 / 0	D3 / 2	D5 / 4	D7 / 6
00H		11	10	01	00									
01H		00	11	10	01									
02H														
03H														
04H														
05H														
06H														
07H														
08H														
09H														
0AH														
0BH														
0CH														
0DH														
0EH														
0FH														
10H														
11H														
12H														
13H														
14H														
15H														
16H														
17H														
18H														
19H														
1AH														
1BH														
		Page_C0				Page_C1					Page_C31			
6CH														
6DH														
6EH														
6FH														
70H														
71H														
72H														
73H														
74H														
75H														
76H														
77H														
78H														
79H														
7AH														
7BH														
7CH														
7DH														
7EH														
7FH														

MX														
	0	C1	C2	C3	C4	C5	C6	C7	C8		C125	C126	C127	C128
	1	C128	C127	C126	C125	C124	C123	C122	C121		C4	C3	C2	C1

Line Adderss	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H	R1	R113	R128	R16
01H	R2	R114	R127	R15
02H	R3	R115	R126	R14
03H	R4	R116	R125	R13
04H	R5	R117	R124	R12
05H	R6	R118	R123	R11
06H	R7	R19	R122	R10
07H	R8	R120	R121	R9
08H	R9	R121	R120	R8
09H	R10	R122	R119	R7
0AH	R11	R123	R118	R6
0BH	R12	R124	R117	R5
0CH	R13	R125	R116	R4
0DH	R14	R126	R115	R3
0EH	R15	R127	R114	R2
0FH	R16	R128	R113	R1
10H	R17	R1	R112	R128
11H	R18	R2	R111	R127
12H	R19	R3	R110	R126
13H	R20	R4	R109	R125
14H	R21	R5	R108	R124
15H	R22	R6	R107	R123
16H	R23	R7	R106	R122
17H	R24	R8	R105	R121
18H	R25	R9	R104	R120
19H	R26	R10	R103	R119
1AH	R27	R11	R102	R118
1BH	R28	R12	R101	R117
6CH	R109	R93	R20	R36
6DH	R110	R94	R19	R35
6EH	R111	R95	R18	R34
6FH	R112	R96	R17	R33
70H	R113	R97	R16	R32
71H	R114	R98	R15	R31
72H	R115	R99	R14	R30
73H	R116	R100	R13	R29
74H	R117	R101	R12	R28
75H	R118	R102	R11	R27
76H	R119	R103	R10	R26
77H	R120	R104	R9	R25
78H	R121	R105	R8	R24
79H	R122	R106	R7	R23
7AH	R123	R107	R6	R22
7BH	R124	R108	R5	R21
7CH	R125	R109	R4	R20
7DH	R126	R110	R3	R19
7EH	R127	R111	R2	R18
7FH	R128	R112	R1	R17
			128	128
			MUX	

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

Row1 Page_C0 ⇨ D[7:0] : 00011011b

Row2 Page_C0 ⇨ D[7:0] : 01101100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1617s has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1617s enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1617s has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

OM changes are synchronized with the edges of UC1617s internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` *or* `System Reset` commands.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1617s consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1617s contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1617s internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1617s power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of `System-Reset` command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1617s. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

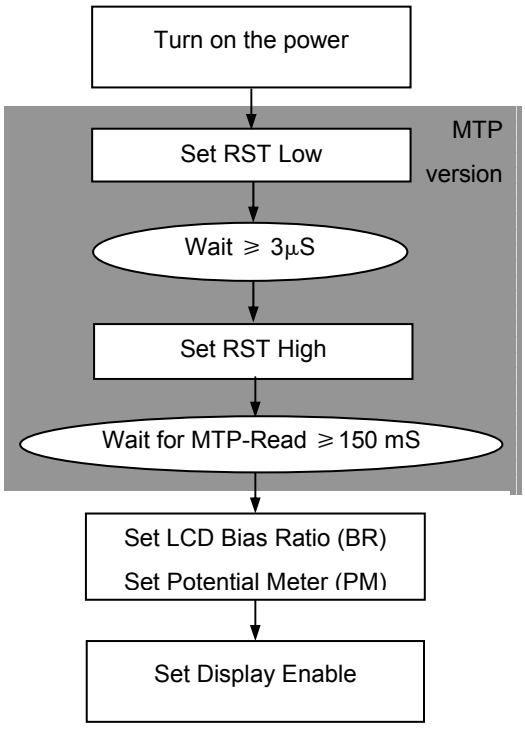


Figure 10: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 330nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1617s will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

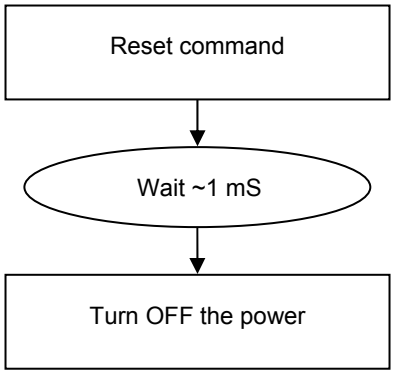


Figure 11: Reference Power-Down Sequence

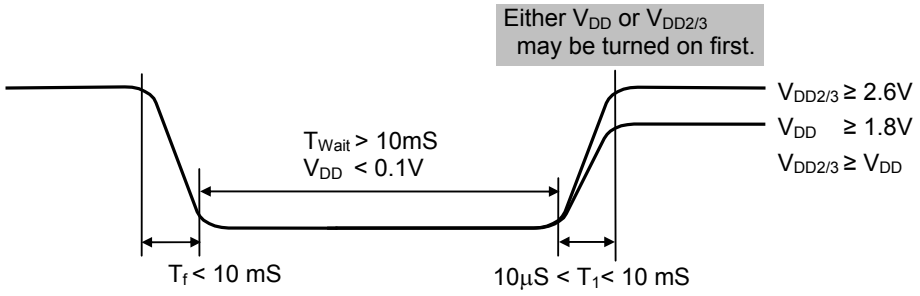


Figure 12: Delay allowance between V_{DD} and V_{DD23}

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1617s such that 1LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1617s:

MTP-Erase, MTP-Program, MTP-Read.

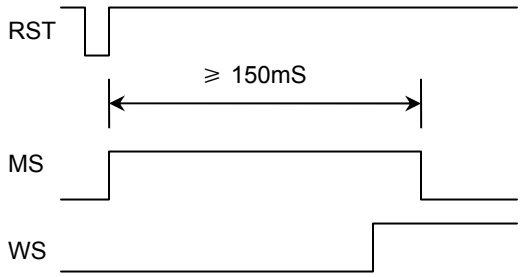
MTP-Program requires an external power source supplied to the TST4 pin. MTP allows program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1617s, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1617s, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the `Read Status` commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use `Read Status` command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the normal operation, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software RESET command. This enables the ICs to turn on display faster without the delay caused by MTP-Read.

It is recommended to use the software *RESET* for such operation control purpose and use hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to V_{DD3}.

	V_{LCD}	**TST4 (external input)**
Program	MTP3 : 39h (12V)	10V (1mA per bit)
Erase	MTP3 : 39h (12V)	Floating or V_{DD3}
Read	MTP2 : 00h (6V)	Floating or V_{DD3}

Note:

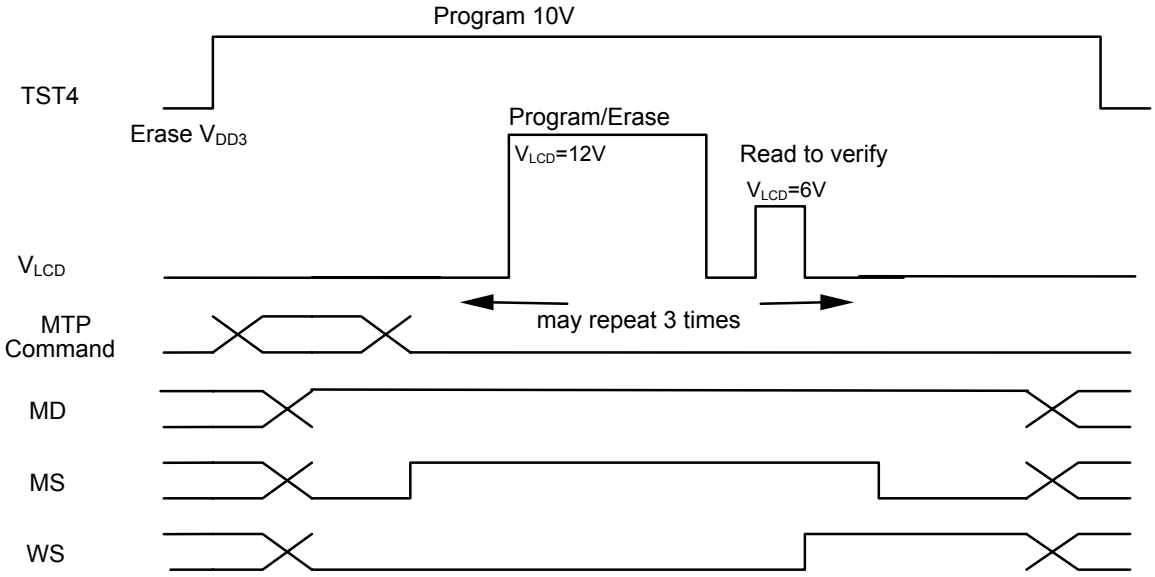
1. Do Erase before Program and Program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqq 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not.

WS : If the operation succeeded, and current operation will be ended with WS=1.
If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted.

MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 8 MTP cell bits. They are divided into two groups for different trimming purpose.

(1) MTP[5:0] : V_{LCD} Trim

When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

(2) MTP[7:6] : For LCM manufacturer's configuration.

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP VLCD
R	0	0	0	0	1	1	1	0	0	1		MTP3: 39h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	1	1		MTP4: 27h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	0		MTP5: 04h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	-	-	0	0	0	0	0	1	MTPM	Ex: To program D0 to be 1, set MTPM to 000001b*
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP3: 39h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	1	1		MTP4: 27h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	0		MTP5: 04h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	-	-	1	1	1	1	1	1	MTPM	Ex: To erase D[7:0], set MTPM to 111111b*
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R											V_{DD}=0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1).
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait3μS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait 150mS after V_{DD} is ON
R	0 0	0 0	0 0	0 0	1 0	1 0	0 0	0 0	0 0	1 0	Set APC Command	Turn ON low voltage detector function.
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	Set Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1617s require special "ESD Sensitivity" consideration in particular:

Test Mode (normal samples – MTP:00)		MM*		HBM*	
		V_{DD} mode	V_{SS} mode	V_{DD} mode	V_{SS} mode
LCD Driver		200V	200V	2.5KV	2.5KV
LCM Digital Interface		300V	300V	3.0KV	3.0KV
LCM HV pin/ Test pin	TST1/2/4	250V	250V	3.0KV	2.5KV
	CB pins	300V	300V	3.0KV	3.0KV
	VLCDIN	300V	300V	3.0KV	3.0KV
	VLCDOUT	300V	300V	3.0KV	3.0KV
PWR / GND			300V		3.0KV

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage (-30^{O}C ~ +80^{O}C)	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.6		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.6V$, 25°C		14	15	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.6V$, 25°C	0.89		1.78	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3} = 3.3V$, Temp = 85 °C			50	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ONS(COM)}$	Downward COM output impedance			1.85	2.5	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	21.1	+10%	kHz

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 14 V,
Mux Rate = 128,
C_B = 2.2 μF,
All HV outputs are open circuit.

Bias Ratio = 11,
Line Rate = 00 b,
Bus mode = 6800,
Temperature = 25°C,

PM = 78,
Panel Loading (PC[1:0]) = 10b,
C_L = 330 nF,
MTP = 00 H,

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	435	653
2-pixel checker	Bus = idle	462	693
-	Reset (standby current)	< 1	5

AC CHARACTERISTICS

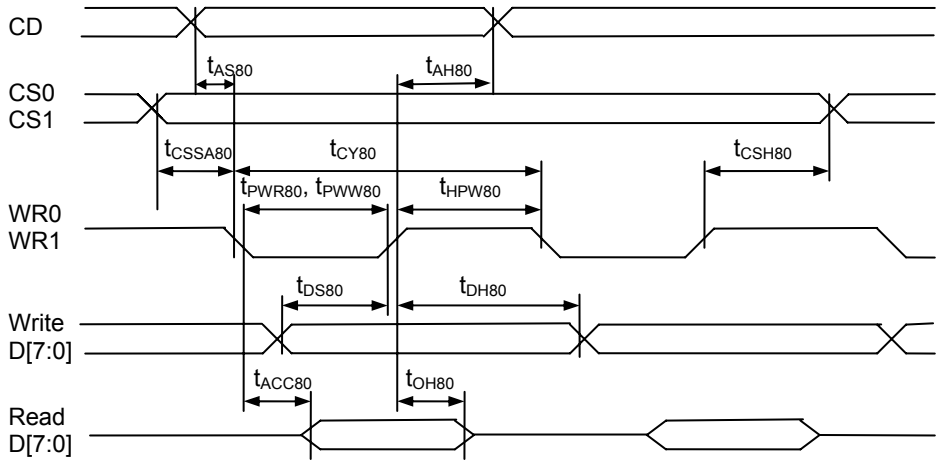


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.465V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		170 130	–	nS
t_{PWR80}	WR1	Pulse width (read)		85	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		85 65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	65 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		320 270	–	nS
t_{PWR80}	WR1	Pulse width (read)		160	–	nS
t_{PWW80}	WR0	Pulse width (write)		135	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		160 135	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	120 60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

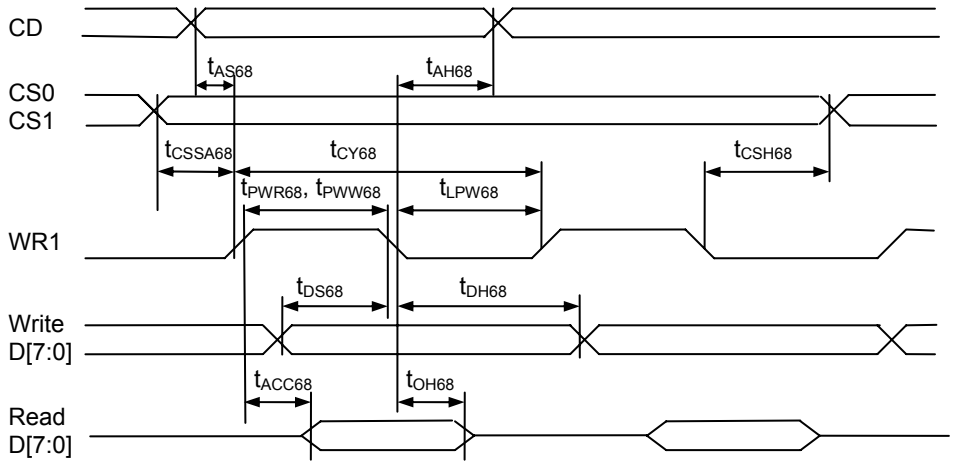


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ⩽ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time (read) (write)		170 130	–	nS
t_{PWR68}	WR1	Pulse width (read)		85	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width (read) (write)		85 65	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OH68}		Read access time Output disable time	C_L = 100pF	– –	70 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time (read) (write)		320 270	–	nS
t_{PWR68}	WR1	Pulse width (read)		160	–	nS
t_{PWW68}		Pulse width (write)		135	–	nS
t_{LPW68}		Low pulse width (read) (write)		160 135	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OH68}		Read access time Output disable time	C_L = 100pF	– –	120 60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

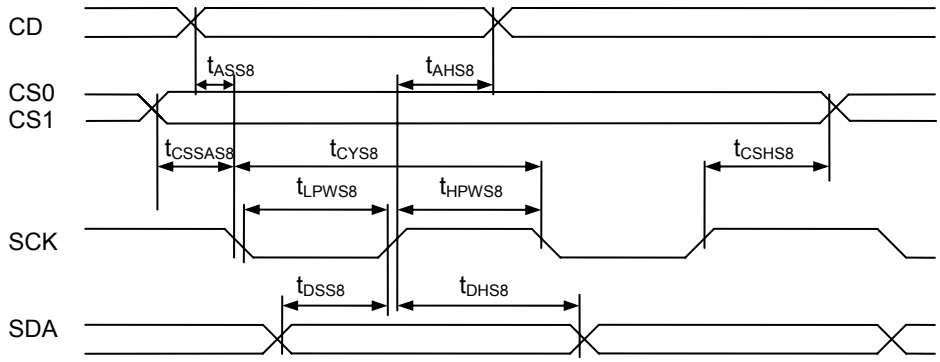


FIGURE 15: Serial Bus Timing Characteristics (for S8)

(2.5V ⩽ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		35	–	nS
t_{LPWS8}		Low pulse width		17	–	nS
t_{HPWS8}		High pulse width		17	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 5	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS
Read:						
t_{CYS8}	SCK	System cycle time		110	–	nS
t_{LPWS8}		Low pulse width		55	–	nS
t_{HPWS8}		High pulse width		55	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time	C_L = 100pF	– N/A	50 N/A	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		60	–	nS
t_{LPWS8}		Low pulse width		30	–	nS
t_{HPWS8}		High pulse width		30	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		24 5	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS
Read:						
t_{CYS8}	SCK	System cycle time		185	–	nS
t_{LPWS8}		Low pulse width		92	–	nS
t_{HPWS8}		High pulse width		92	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time	C_L = 100pF	– N/A	90 N/A	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

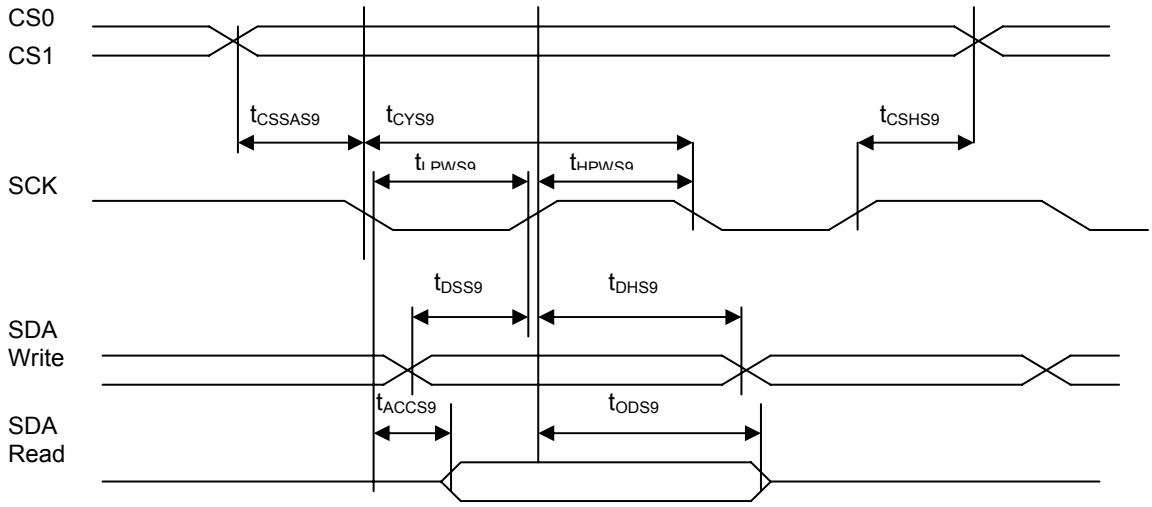


FIGURE 16: Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.465V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{CYS9}	SCK	System cycle time		35	–	nS
t_{LPWS9}		Low pulse width		17	–	nS
t_{HPWS9}		High pulse width		17	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 5	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS
Read:						
t_{CYS9}	SCK	System cycle time		110	–	nS
t_{LPWS9}		Low pulse width		55	–	nS
t_{HPWS9}		High pulse width		55	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time	C_L = 100pF	– N/A	50 N/A	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{CYS9}	SCK	System cycle time		60	–	nS
t_{LPWS9}		Low pulse width		30	–	nS
t_{HPWS9}		High pulse width		30	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		24 5	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS
Read:						
t_{CYS9}	SCK	System cycle time		185	–	nS
t_{LPWS9}		Low pulse width		92	–	nS
t_{HPWS9}		High pulse width		92	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time	C_L = 100pF	– N/A	90 N/A	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

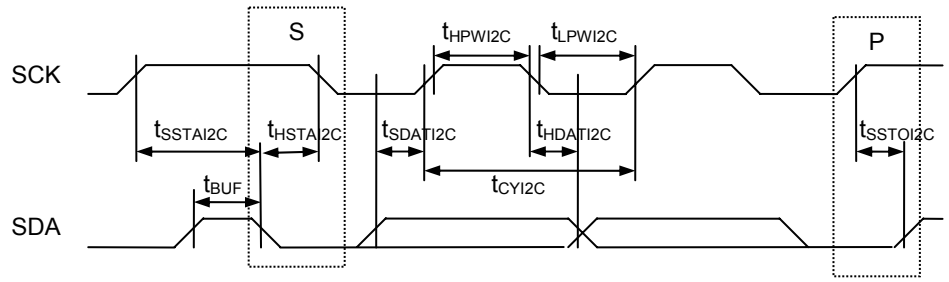


FIGURE 16: Serial bus timing characteristics (for I^2C)

($2.5V \leqslant V_{DD} < 3.465V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ⩽ 100nS	580 275	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		290 137	–	nS
t_{HPWI2C}		High pulse width (read) (write)		290 137	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		28	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		28	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		165	–	nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ⩽ 100nS	750 330	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		375 165	–	nS
t_{HPWI2C}		High pulse width (read) (write)		375 165	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		55	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		60	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		220		nS

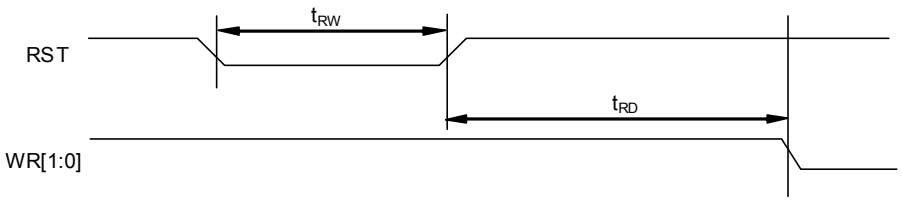


FIGURE 17: Reset Characteristics

(1.65V ⩽ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
6582 x 870 ± 40 μM^2

DIE THICKNESS:
400 ± 20 μM

BUMP HEIGHT:
15 ± 3 μM
(H_{MAX} - H_{MIN}) within die ⩽ 2 μM

COM/SEG SIZE:
138 x 14.5 μM^2 (Typ.)

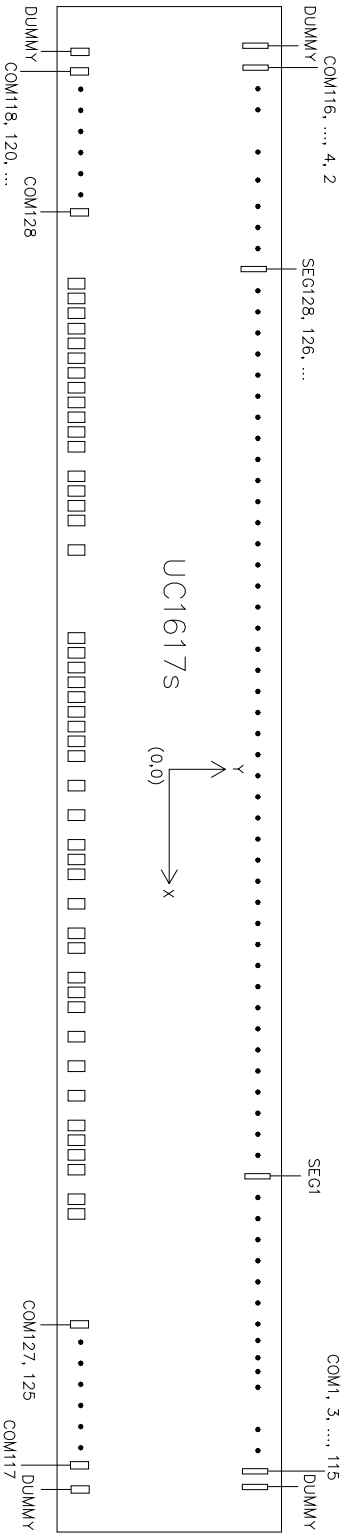
BUMP PITCH:
26.5 μM

BUMP GAP:
12 μM (Typ.)

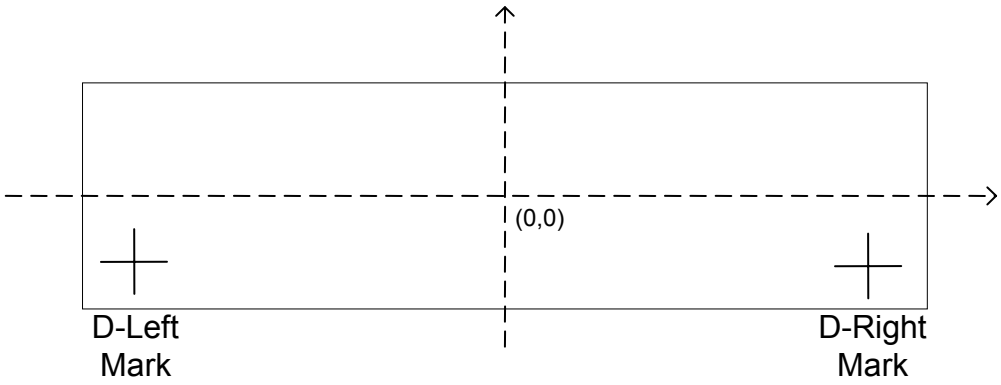
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

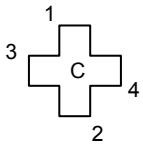
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

The “x” and “+” marks are symmetric both horizontally and vertically.

COORDINATES:

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-3024	-332.5	3004	-332.5
2	-3004	-392.5	3024	-392.5
3	-3044	-352.5	2984	-352.5
4	-2984	-372.5	3044	-372.5
C	-3014	-362.5	3014	-362.5

TOP METAL AND PASSIVATION:

FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-3246.25	-331.5	14.5	138
2	COM118	-3219.75	-331.5	14.5	138
3	COM120	-3193.25	-331.5	14.5	138
4	COM122	-3166.75	-331.5	14.5	138
5	COM124	-3140.25	-331.5	14.5	138
6	COM126	-3113.75	-331.5	14.5	138
7	COM128	-3087.25	-331.5	14.5	138
8	D0	-2923.95	-349.5	70	100
9	D1	-2838.85	-349.5	70	100
10	D2	-2753.75	-349.5	70	100
11	D3	-2668.65	-349.5	70	100
12	D4	-2583.55	-349.5	70	100
13	D5	-2498.45	-349.5	70	100
14	D6	-2413.35	-349.5	70	100
15	VDDX	-2341.8	-349.5	25	100
16	D7	-2270.25	-349.5	70	100
17	RST_	-2179.9	-349.5	66.5	100
18	CS0	-2098.3	-349.5	66.5	100
19	VDDX	-2028.5	-349.5	25	100
20	CS1	-1958.7	-349.5	66.5	100
21	CD	-1877.1	-349.5	66.5	100
22	WR0	-1795.5	-349.5	66.5	100
23	VDDX	-1725.7	-349.5	25	100
24	WR1	-1655.9	-349.5	66.5	100
25	TST4	-1576.1	-349.5	45	100
26	TST4	-1516.1	-349.5	45	100
27	TST1	-1080.225	-349.5	45	100
28	BM0	-1000.3	-349.5	66.5	100
29	VDDX	-930.5	-349.5	25	100
30	BM1	-860.7	-349.5	66.5	100
31	TST2	-780.025	-349.5	45	100
32	ID	-604.575	-349.5	66.5	100
33	VDDX	-524.775	-349.5	45	100
34	VSS	-464.775	-349.5	45	100
35	VSS	-404.775	-349.5	45	100
36	VSS	-344.775	-349.5	45	100
37	VSS	-284.775	-349.5	45	100
38	VSS2	-111.775	-349.5	45	100
39	VSS2	-51.775	-349.5	45	100
40	VSS2	8.225	-349.5	45	100
41	VSS2	68.225	-349.5	45	100
42	VSS2	128.225	-349.5	45	100
43	VDD3	188.225	-349.5	45	100
44	DUMMY	366.575	-349.5	51	100
45	VDD2	453.075	-349.5	45	100
46	VDD2	513.075	-349.5	45	100
47	DUMMY	678	-349.5	51	100
48	DUMMY	744	-349.5	51	100
49	DUMMY	810	-349.5	51	100
50	DUMMY	876	-349.5	51	100
51	DUMMY	942	-349.5	51	100
52	DUMMY	1008	-349.5	51	100
53	DUMMY	1074	-349.5	51	100
54	DUMMY	1140	-349.5	51	100
55	VDD	1304.925	-349.5	45	100
56	VB0+	1412.1	-349.5	45	100
57	VB0+	1472.1	-349.5	45	100
58	VB1+	1688.6	-349.5	45	100
59	VB1+	1748.6	-349.5	45	100
60	VB1-	2103.6	-349.5	45	100
61	VB1-	2163.6	-349.5	45	100

#	Pad	X	Y	W	H
62	VB0-	2379.3	-349.5	45	100
63	VB0-	2439.3	-349.5	45	100
64	VLCDIN	2655	-349.5	45	100
65	VLCDOUT	2715	-349.5	45	100
66	COM127	3087.25	-331.5	14.5	138
67	COM125	3113.75	-331.5	14.5	138
68	COM123	3140.25	-331.5	14.5	138
69	COM121	3166.75	-331.5	14.5	138
70	COM119	3193.25	-331.5	14.5	138
71	COM117	3219.75	-331.5	14.5	138
72	DUMMY	3246.25	-331.5	14.5	138
73	DUMMY	3246.25	331.5	14.5	138
74	COM115	3219.75	331.5	14.5	138
75	COM113	3193.25	331.5	14.5	138
76	COM111	3166.75	331.5	14.5	138
77	COM109	3140.25	331.5	14.5	138
78	COM107	3113.75	331.5	14.5	138
79	COM105	3087.25	331.5	14.5	138
80	COM103	3060.75	331.5	14.5	138
81	COM101	3034.25	331.5	14.5	138
82	COM99	3007.75	331.5	14.5	138
83	COM97	2981.25	331.5	14.5	138
84	COM95	2954.75	331.5	14.5	138
85	COM93	2928.25	331.5	14.5	138
86	COM91	2901.75	331.5	14.5	138
87	COM89	2875.25	331.5	14.5	138
88	COM87	2848.75	331.5	14.5	138
89	COM85	2822.25	331.5	14.5	138
90	COM83	2795.75	331.5	14.5	138
91	COM81	2769.25	331.5	14.5	138
92	COM79	2742.75	331.5	14.5	138
93	COM77	2716.25	331.5	14.5	138
94	COM75	2689.75	331.5	14.5	138
95	COM73	2663.25	331.5	14.5	138
96	COM71	2636.75	331.5	14.5	138
97	COM69	2610.25	331.5	14.5	138
98	COM67	2583.75	331.5	14.5	138
99	COM65	2557.25	331.5	14.5	138
100	COM63	2530.75	331.5	14.5	138
101	COM61	2504.25	331.5	14.5	138
102	COM59	2477.75	331.5	14.5	138
103	COM57	2451.25	331.5	14.5	138
104	COM55	2424.75	331.5	14.5	138
105	COM53	2398.25	331.5	14.5	138
106	COM51	2371.75	331.5	14.5	138
107	COM49	2345.25	331.5	14.5	138
108	COM47	2318.75	331.5	14.5	138
109	COM45	2292.25	331.5	14.5	138
110	COM43	2265.75	331.5	14.5	138
111	COM41	2239.25	331.5	14.5	138
112	COM39	2212.75	331.5	14.5	138
113	COM37	2186.25	331.5	14.5	138
114	COM35	2159.75	331.5	14.5	138
115	COM33	2133.25	331.5	14.5	138
116	COM31	2106.75	331.5	14.5	138
117	COM29	2080.25	331.5	14.5	138
118	COM27	2053.75	331.5	14.5	138
119	COM25	2027.25	331.5	14.5	138
120	COM23	2000.75	331.5	14.5	138
121	COM21	1974.25	331.5	14.5	138
122	COM19	1947.75	331.5	14.5	138

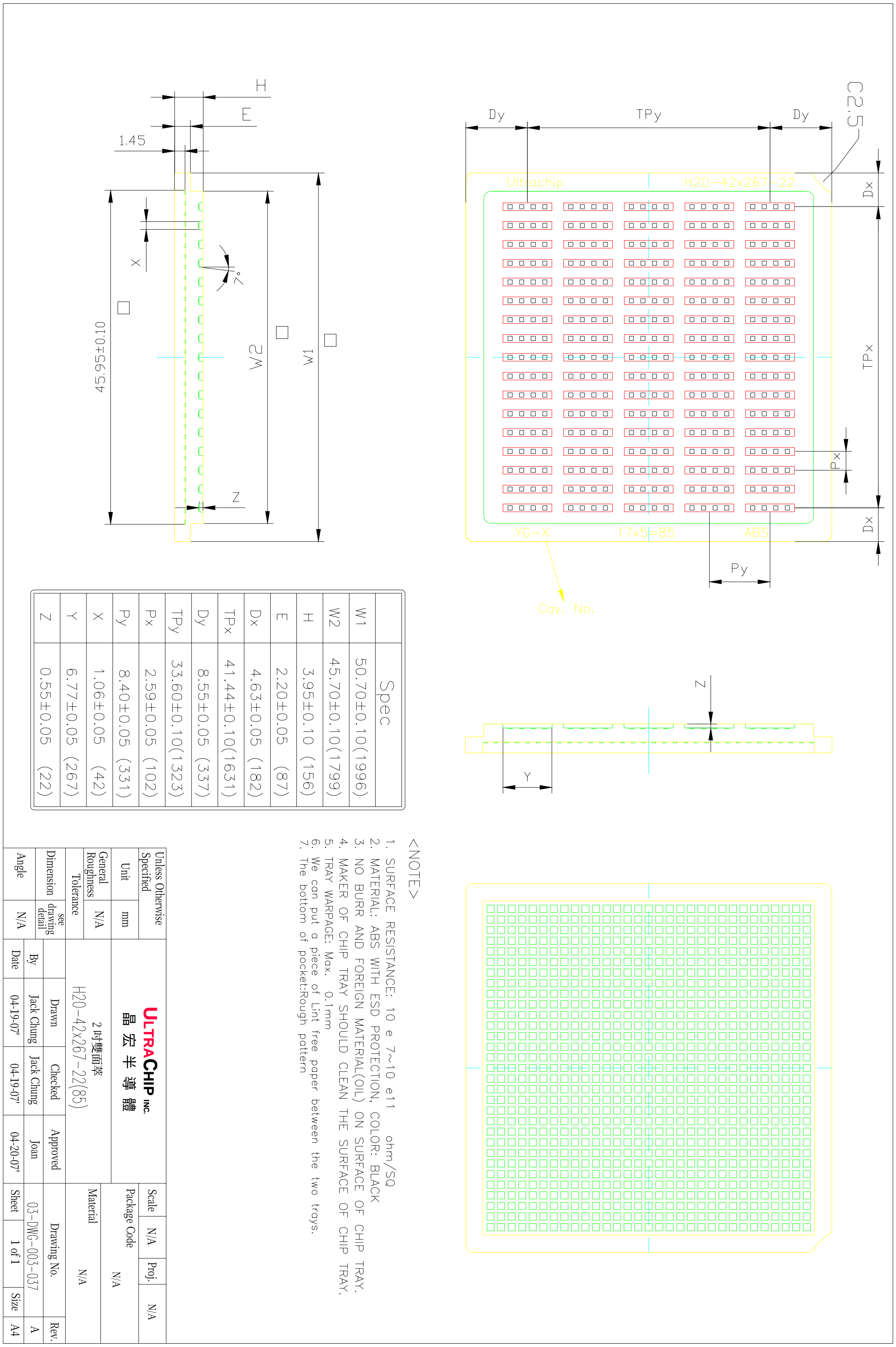
#	Pad	X	Y	W	H
123	COM17	1921.25	331.5	14.5	138
124	COM15	1894.75	331.5	14.5	138
125	COM13	1868.25	331.5	14.5	138
126	COM11	1841.75	331.5	14.5	138
127	COM9	1815.25	331.5	14.5	138
128	COM7	1788.75	331.5	14.5	138
129	COM5	1762.25	331.5	14.5	138
130	COM3	1735.75	331.5	14.5	138
131	COM1	1709.25	331.5	14.5	138
132	SEG1	1682.75	331.5	14.5	138
133	SEG2	1656.25	331.5	14.5	138
134	SEG3	1629.75	331.5	14.5	138
135	SEG4	1603.25	331.5	14.5	138
136	SEG5	1576.75	331.5	14.5	138
137	SEG6	1550.25	331.5	14.5	138
138	SEG7	1523.75	331.5	14.5	138
139	SEG8	1497.25	331.5	14.5	138
140	SEG9	1470.75	331.5	14.5	138
141	SEG10	1444.25	331.5	14.5	138
142	SEG11	1417.75	331.5	14.5	138
143	SEG12	1391.25	331.5	14.5	138
144	SEG13	1364.75	331.5	14.5	138
145	SEG14	1338.25	331.5	14.5	138
146	SEG15	1311.75	331.5	14.5	138
147	SEG16	1285.25	331.5	14.5	138
148	SEG17	1258.75	331.5	14.5	138
149	SEG18	1232.25	331.5	14.5	138
150	SEG19	1205.75	331.5	14.5	138
151	SEG20	1179.25	331.5	14.5	138
152	SEG21	1152.75	331.5	14.5	138
153	SEG22	1126.25	331.5	14.5	138
154	SEG23	1099.75	331.5	14.5	138
155	SEG24	1073.25	331.5	14.5	138
156	SEG25	1046.75	331.5	14.5	138
157	SEG26	1020.25	331.5	14.5	138
158	SEG27	993.75	331.5	14.5	138
159	SEG28	967.25	331.5	14.5	138
160	SEG29	940.75	331.5	14.5	138
161	SEG30	914.25	331.5	14.5	138
162	SEG31	887.75	331.5	14.5	138
163	SEG32	861.25	331.5	14.5	138
164	SEG33	834.75	331.5	14.5	138
165	SEG34	808.25	331.5	14.5	138
166	SEG35	781.75	331.5	14.5	138
167	SEG36	755.25	331.5	14.5	138
168	SEG37	728.75	331.5	14.5	138
169	SEG38	702.25	331.5	14.5	138
170	SEG39	675.75	331.5	14.5	138
171	SEG40	649.25	331.5	14.5	138
172	SEG41	622.75	331.5	14.5	138
173	SEG42	596.25	331.5	14.5	138
174	SEG43	569.75	331.5	14.5	138
175	SEG44	543.25	331.5	14.5	138
176	SEG45	516.75	331.5	14.5	138
177	SEG46	490.25	331.5	14.5	138
178	SEG47	463.75	331.5	14.5	138
179	SEG48	437.25	331.5	14.5	138
180	SEG49	410.75	331.5	14.5	138
181	SEG50	384.25	331.5	14.5	138
182	SEG51	357.75	331.5	14.5	138
183	SEG52	331.25	331.5	14.5	138
184	SEG53	304.75	331.5	14.5	138
185	SEG54	278.25	331.5	14.5	138
186	SEG55	251.75	331.5	14.5	138

#	Pad	X	Y	W	H
187	SEG56	225.25	331.5	14.5	138
188	SEG57	198.75	331.5	14.5	138
189	SEG58	172.25	331.5	14.5	138
190	SEG59	145.75	331.5	14.5	138
191	SEG60	119.25	331.5	14.5	138
192	SEG61	92.75	331.5	14.5	138
193	SEG62	66.25	331.5	14.5	138
194	SEG63	39.75	331.5	14.5	138
195	SEG64	13.25	331.5	14.5	138
196	SEG65	-13.25	331.5	14.5	138
197	SEG66	-39.75	331.5	14.5	138
198	SEG67	-66.25	331.5	14.5	138
199	SEG68	-92.75	331.5	14.5	138
200	SEG69	-119.25	331.5	14.5	138
201	SEG70	-145.75	331.5	14.5	138
202	SEG71	-172.25	331.5	14.5	138
203	SEG72	-198.75	331.5	14.5	138
204	SEG73	-225.25	331.5	14.5	138
205	SEG74	-251.75	331.5	14.5	138
206	SEG75	-278.25	331.5	14.5	138
207	SEG76	-304.75	331.5	14.5	138
208	SEG77	-331.25	331.5	14.5	138
209	SEG78	-357.75	331.5	14.5	138
210	SEG79	-384.25	331.5	14.5	138
211	SEG80	-410.75	331.5	14.5	138
212	SEG81	-437.25	331.5	14.5	138
213	SEG82	-463.75	331.5	14.5	138
214	SEG83	-490.25	331.5	14.5	138
215	SEG84	-516.75	331.5	14.5	138
216	SEG85	-543.25	331.5	14.5	138
217	SEG86	-569.75	331.5	14.5	138
218	SEG87	-596.25	331.5	14.5	138
219	SEG88	-622.75	331.5	14.5	138
220	SEG89	-649.25	331.5	14.5	138
221	SEG90	-675.75	331.5	14.5	138
222	SEG91	-702.25	331.5	14.5	138
223	SEG92	-728.75	331.5	14.5	138
224	SEG93	-755.25	331.5	14.5	138
225	SEG94	-781.75	331.5	14.5	138
226	SEG95	-808.25	331.5	14.5	138
227	SEG96	-834.75	331.5	14.5	138
228	SEG97	-861.25	331.5	14.5	138
229	SEG98	-887.75	331.5	14.5	138
230	SEG99	-914.25	331.5	14.5	138
231	SEG100	-940.75	331.5	14.5	138
232	SEG101	-967.25	331.5	14.5	138
233	SEG102	-993.75	331.5	14.5	138
234	SEG103	-1020.25	331.5	14.5	138
235	SEG104	-1046.75	331.5	14.5	138
236	SEG105	-1073.25	331.5	14.5	138
237	SEG106	-1099.75	331.5	14.5	138
238	SEG107	-1126.25	331.5	14.5	138
239	SEG108	-1152.75	331.5	14.5	138
240	SEG109	-1179.25	331.5	14.5	138
241	SEG110	-1205.75	331.5	14.5	138
242	SEG111	-1232.25	331.5	14.5	138
243	SEG112	-1258.75	331.5	14.5	138
244	SEG113	-1285.25	331.5	14.5	138
245	SEG114	-1311.75	331.5	14.5	138
246	SEG115	-1338.25	331.5	14.5	138
247	SEG116	-1364.75	331.5	14.5	138
248	SEG117	-1391.25	331.5	14.5	138
249	SEG118	-1417.75	331.5	14.5	138
250	SEG119	-1444.25	331.5	14.5	138

#	Pad	X	Y	W	H
251	SEG120	-1470.75	331.5	14.5	138
252	SEG121	-1497.25	331.5	14.5	138
253	SEG122	-1523.75	331.5	14.5	138
254	SEG123	-1550.25	331.5	14.5	138
255	SEG124	-1576.75	331.5	14.5	138
256	SEG125	-1603.25	331.5	14.5	138
257	SEG126	-1629.75	331.5	14.5	138
258	SEG127	-1656.25	331.5	14.5	138
259	SEG128	-1682.75	331.5	14.5	138
260	COM2	-1709.25	331.5	14.5	138
261	COM4	-1735.75	331.5	14.5	138
262	COM6	-1762.25	331.5	14.5	138
263	COM8	-1788.75	331.5	14.5	138
264	COM10	-1815.25	331.5	14.5	138
265	COM12	-1841.75	331.5	14.5	138
266	COM14	-1868.25	331.5	14.5	138
267	COM16	-1894.75	331.5	14.5	138
268	COM18	-1921.25	331.5	14.5	138
269	COM20	-1947.75	331.5	14.5	138
270	COM22	-1974.25	331.5	14.5	138
271	COM24	-2000.75	331.5	14.5	138
272	COM26	-2027.25	331.5	14.5	138
273	COM28	-2053.75	331.5	14.5	138
274	COM30	-2080.25	331.5	14.5	138
275	COM32	-2106.75	331.5	14.5	138
276	COM34	-2133.25	331.5	14.5	138
277	COM36	-2159.75	331.5	14.5	138
278	COM38	-2186.25	331.5	14.5	138
279	COM40	-2212.75	331.5	14.5	138
280	COM42	-2239.25	331.5	14.5	138
281	COM44	-2265.75	331.5	14.5	138
282	COM46	-2292.25	331.5	14.5	138
283	COM48	-2318.75	331.5	14.5	138
284	COM50	-2345.25	331.5	14.5	138
285	COM52	-2371.75	331.5	14.5	138
286	COM54	-2398.25	331.5	14.5	138
287	COM56	-2424.75	331.5	14.5	138
288	COM58	-2451.25	331.5	14.5	138
289	COM60	-2477.75	331.5	14.5	138
290	COM62	-2504.25	331.5	14.5	138

#	Pad	X	Y	W	H
291	COM64	-2530.75	331.5	14.5	138
292	COM66	-2557.25	331.5	14.5	138
293	COM68	-2583.75	331.5	14.5	138
294	COM70	-2610.25	331.5	14.5	138
295	COM72	-2636.75	331.5	14.5	138
296	COM74	-2663.25	331.5	14.5	138
297	COM76	-2689.75	331.5	14.5	138
298	COM78	-2716.25	331.5	14.5	138
299	COM80	-2742.75	331.5	14.5	138
300	COM82	-2769.25	331.5	14.5	138
301	COM84	-2795.75	331.5	14.5	138
302	COM86	-2822.25	331.5	14.5	138
303	COM88	-2848.75	331.5	14.5	138
304	COM90	-2875.25	331.5	14.5	138
305	COM92	-2901.75	331.5	14.5	138
306	COM94	-2928.25	331.5	14.5	138
307	COM96	-2954.75	331.5	14.5	138
308	COM98	-2981.25	331.5	14.5	138
309	COM100	-3007.75	331.5	14.5	138
310	COM102	-3034.25	331.5	14.5	138
311	COM104	-3060.75	331.5	14.5	138
312	COM106	-3087.25	331.5	14.5	138
313	COM108	-3113.75	331.5	14.5	138
314	COM110	-3140.25	331.5	14.5	138
315	COM112	-3166.75	331.5	14.5	138
316	COM114	-3193.25	331.5	14.5	138
317	COM116	-3219.75	331.5	14.5	138
318	DUMMY	-3246.25	331.5	14.5	138

TRAY INFORMATION



	Spec
W1	50.70±0.10(1996)
W2	45.70±0.10(1799)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	4.63±0.05 (182)
TPx	41.44±0.10(1631)
Dy	8.55±0.05 (337)
TPy	33.60±0.10(1323)
Px	2.59±0.05 (102)
Py	8.40±0.05 (331)
X	1.06±0.05 (42)
Y	6.77±0.05 (267)
Z	0.55±0.05 (22)

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	(First release)	Jul. 19, 2007
0.8	(1) $V_{DD2/3}$ (Typical) Range is adjusted: 2.6V~3.3V → 2.7V~3.3V (Section "Feature Highlight", page 3)	Aug. 22, 2007
	(2) One more byte is inserted as first byte to Get Status Command: 1111 1110 (Section "Command Table" – (41) Get Status, page 14; "Command Description" – (41) Get Status, page 26)	
	(3) V_{LCD} formula is updated. (Section "V_{LCD} Quick Reference", page 28)	
	(4) The RAM table is enriched and its example explanation are corrected. 10010011 → 00111001 (Section "Display Data RAM", page 43)	
	(5) The waiting time for Reset Low is corrected: 1mS → 3uS ... Reset High … : 5~10mS → 150mS (Section "Reset & Power Management" - Figure 10 Power-up Sequence, page 45; "Sample Power Management Command Sequences" – Power-up Table, page 51)	
	(6) V_{LCD} for Program/Erase: MTP3: 3eh(12V) → 39h(12V) (Section "MTP Operation for LCM Makers", page 47; "MTP Command Sequence Sample Code", pages 49, 50)	
	(7) $V_{DD2/3}$ (Min) is adjusted: 2.5 → 2.6V $R_{ON(SEG)}$ (Typ.) : 1.5 → 1.6 kΩ , (Max.) : 2.0 → 2.1 kΩ $R_{ON(COM)}$ is split into 2, Upward and Downward: $R_{ON(COM)}$ Upward (Typ.) : 1.5 → 1.6 kΩ , (Max.) : 2.0 → 2.1 kΩ $R_{ONS(COM)}$ Downward (Typ.) : 1.85 kΩ , (Max.) : 2.5 kΩ (Section "Specification" – DC Characteristics, page 54)	
	(8) The Maximum data present. (Section "Specification" – Power Consumption, page 54)	
	(9) Some AC timings and V_{DD} range are adjusted. (Section "AC Characteristics", Pp 55 ~ 64)	
1.0	(1) Register EF is removed. (Section "Control Register", page 12; "Command Table" – (3)(41) Get Status, pages 13, 14; "Command Description" – (3)(41) Get Status, pages 15, 26)	Aug. 24, 2007